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ESD Protected on-Chip Crystal Oscillator

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Abstract: There are no stand alone on-chip crystal oscillators are available for R&D activities and lab evaluation of a new circuit. The ESD Protected ON-CHIP crystal oscillator is simple and robust to use. It protects itself against any sudden transients that might occur during handling. Thus it is useful for reference designs & electronic Research & Development activities. The On-Chip Crystal Oscillator can be designed by using a layout tool MICROWIND 3.1.7 version. Here the simulation is based on the Tanner Tool.
Also one more feature has been added for use in future to tweak values of Capacitance & Resistance of internal MOSFETS & passive components that might vary. The external input is connected via a digital switching circuit where one can add or bye-pass a few Pico Farads of on chip capacitance and a few ohms of resistance to compensate for stable oscillations.

I. INTRODUCTION:

A Crystal Oscillator is a timing device that consists of a crystal and an oscillator circuit, providing an output waveform at a specific frequency. When a crystal is placed into an amplifier circuit (as shown in Figure1), a small amount of energy is fed back to the crystal, which causes it to vibrate. These vibrations act to stabilize the frequency of the oscillator circuit.

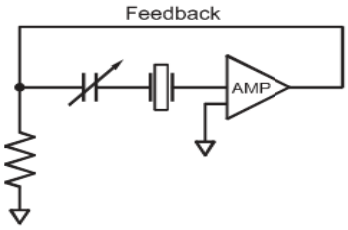


Figure1: Simplified Oscillator Circuit Using a Crystal Resonator

The following diagram Figure2 describes the basic principle of crystal and it's equivalent

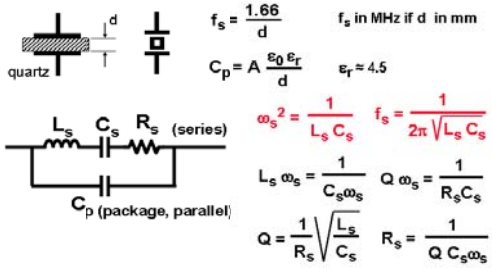


Figure2: Crystal as a Resonator

The ESD Protected ON-CHIP Crystal oscillator with the following Aspects:

i. Electro Static Discharge(ESD)
ii. LATCH-UP Protection

I.Electro static discharge (ESD) is a form of electrical over stress caused by static electricity.
The precautions taken for On-Chip crystal oscillator protected from Electro static discharge(ESD) are

i. Proper handling precautions will minimised the risks of electro static discharge.
ii. ESD sensitive components should always be stored in a static shielded packaging.
iii. Humidifiers, ionizers and antistatic mates can minimize the build-up of static charges around workstations and machinery.
iv. These precautions reduce but do not eliminate ESD damage, so manufacturers routinely include special ESD structures on-board integrated circuit. These structures are design to observe and dissipate moderate levels of ESD energy without damage.

LATCH-UP Protection can cause physical destruction of an IC due to excessive power dissipation and consecutive overheating.The LATCH-UP problem can overcome by introducing of guard rings in the layout.
The block diagram of the proposed system is shown below

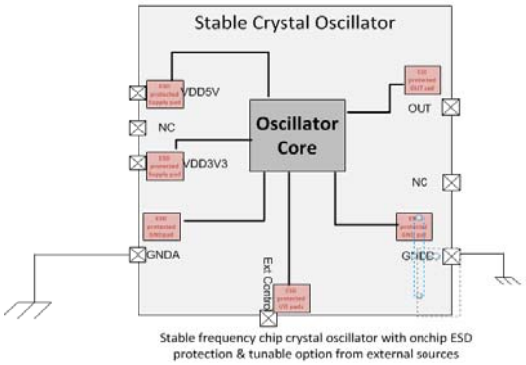


Figure3: On-Chip Crystal Oscillator with ESD protection

Here the Oscillator Core is the Crystal Oscillator to which the ESD protected supply pad, signal pad, ground pad and the input /output pads are externally connected to it.

II.SCHEMATIC DIAGRAM OF THE CRYSTAL OSCILLATOR

The schematic diagram of the proposed crystal oscillator circuit is shown below in the figure

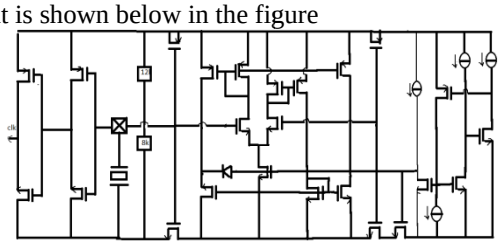


Figure4: Complete Schematic Diagram Of The Crystal Oscillator

III. MICROWIND TOOL:

i. Microwind is a friendly PC tool for designing a circuits at layout level.
ii. The package contains a library of common logic and analog ic's to design.
iii. The tool features various views like 2D cross section, 3D process viewer.

The Complete layout design of the crystal oscillator circuit using microwind tool is shown below in the figure5

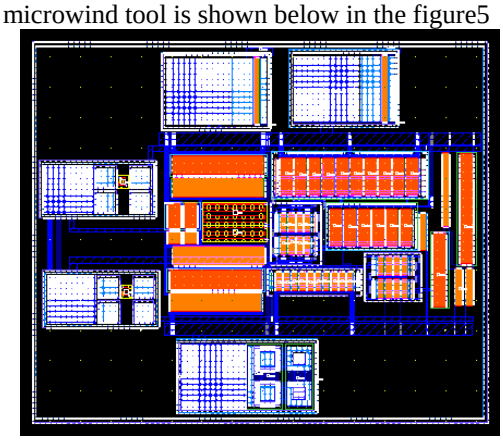


Figure5: Layout Diagram Of The Crystal Oscillator Circuit

ISSUES IN ANALOG LAYOUT:

The layout is the representation of a circuit in the physical domain.

It must contain all the information required to generate the masks for circuit fabrication.

The physical mask layout of any circuit to be manufactured using a particular process must confirm to a set of geometric constraints or rules, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and poly silicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features.

a) DESIGN RULES:

The design rules are usually described in two ways:

Micron rules,in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers,or,

Lambda rules,which specify the layout constraints in terms of a single parameter(lambda) and thus allow linear, proportional scaling of all geometrical constraints.

b) Matching of Devices:

Matching is important because most analog circuit designs use a ratio based design techniques (e.g. current mirrors).

Some common techniques that help improve device matching are MULTI-GATE FINGER LAYOUT and COMMON-CENTROID LAYOUT.

FINGERING:

Analog transistor often having large W/L Use identical finger geometries. . Transistors of different widths and lengths match very poorly. Even minimally matched devices must have identical channel lengths Most matched transistors require relatively large widths and are usually divided into sections , or fingers. Each of these fingers should have the same width and length as all others. The pattern of the fingering is shown below in the Figure6

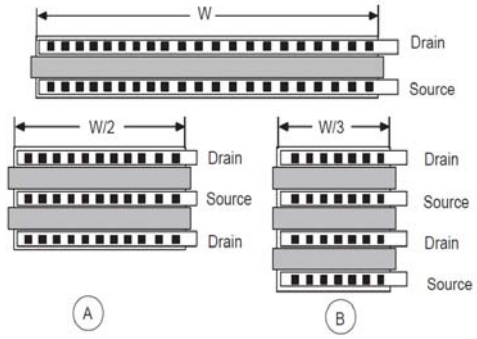


Figure6: Pattern of the Fingering

COMMON CENTROID:

Common-Centroid layout design guidelines:

a. Placement: The geometric center of the devices to match must be very near.
b. Symmetry: The layout of the devices must be evenly distributed in both directions: x and y.
c. Regularity: Partial devices must be distributes uniformly.
d. Dispersion: The layout must be as compact and square as possible.
e. Orientation: The number of partial devices oriented in each direction must be the same for each device to be match.

The diagram for the common centroid technique is shown below:

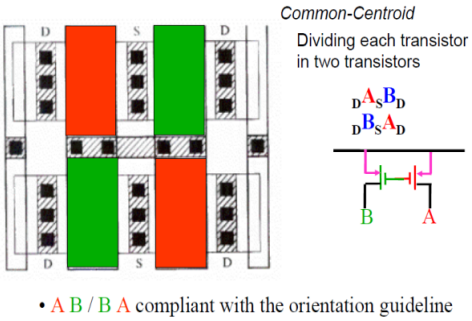


Figure7: Common-Centroid Technique

c) DUMMY RESISTORS

In order to minimize the noise, resistor can be designed

a) with a guard ring
b) inside a well to reduce the coupling to the substrate.

The dummy resistor pattern is shown in the following Figure8

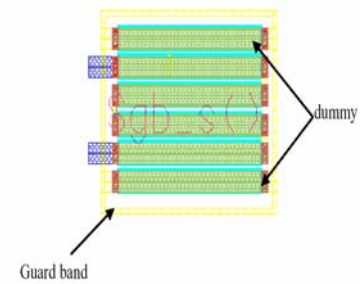


Figure8: Dummy Resistor Pattern

IV. TANNER TOOL:

Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow to enter schematic, perform SPICE simulations.

There are 3 tools that are used for this process:

S-edit - a schematic capture tool

T-SPICE – the SPICE simulation engine integrated with S-edit

L-edit - the physical design tool

The crystal oscillator schematic involves the basic analogue building blocks.

They are:

- Inverter
- Buffer
- Operational amplifier
- Current sources.
- Basic ESD structure
- Input pad block with ESD structure
- Output pad with ESD structure

The schematic diagram of CMOS Inverter drawn in the tanner tool is shown in the figure9 below

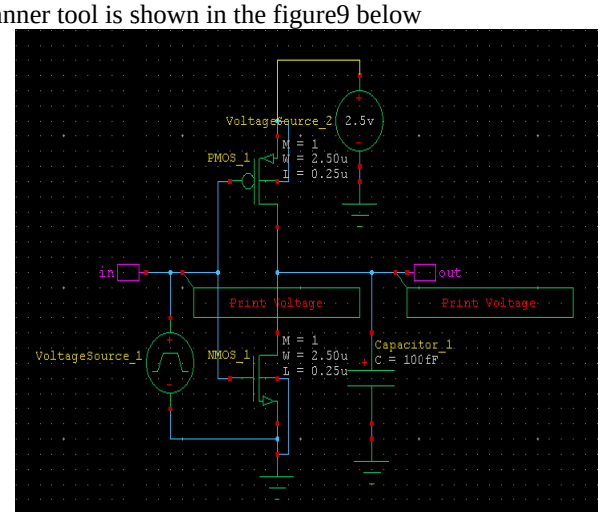


Figure9: Schematic of the Inverter

If any errors or warnings are there then it will be shown at the bottom

After click on the simulator the T-Spice window will appear. If everything is ok, the waveform viewer will also appear. If everything worked , the waveforms should look like this

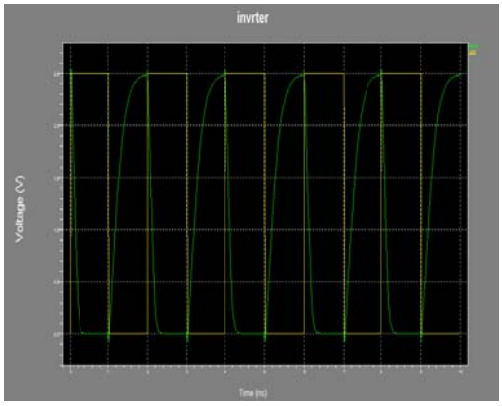


Figure9(a): waveforms of the Inverter

The schematic diagram of the Current mirror in the tanner tool is shown below

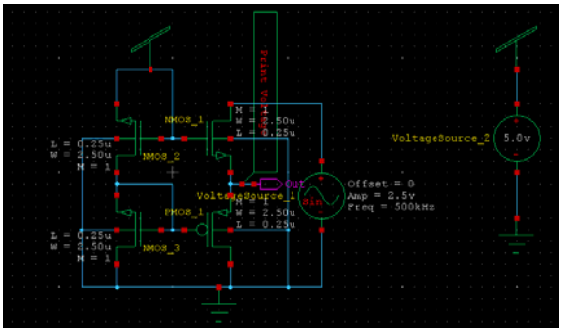


Figure10: Schematic of the Current Mirror

The obtained waveforms for the current mirror are shown below:

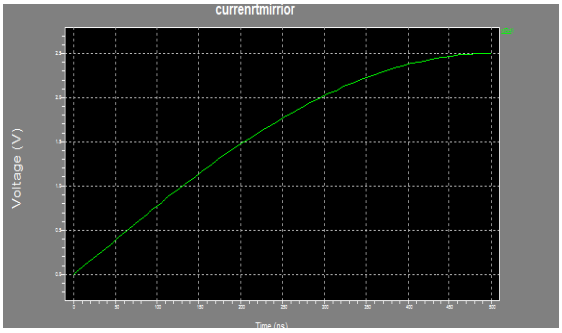


Figure10(a): Waveforms Of the Current mirror

VIEW THE NET LIST:

To see the net list in the T-SPICE window, right click on the file at the bottom and select " show net list. "

This is a good place to look when you get errors. This is the text based description of what we have entered in S-edit.

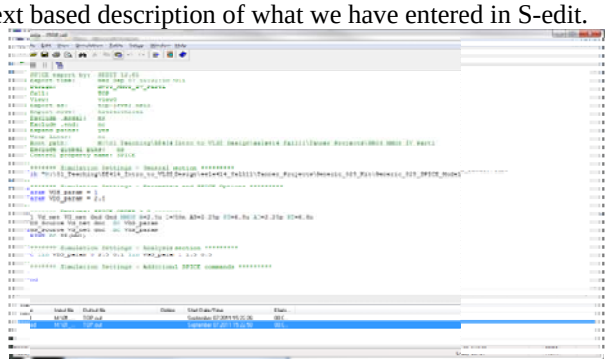
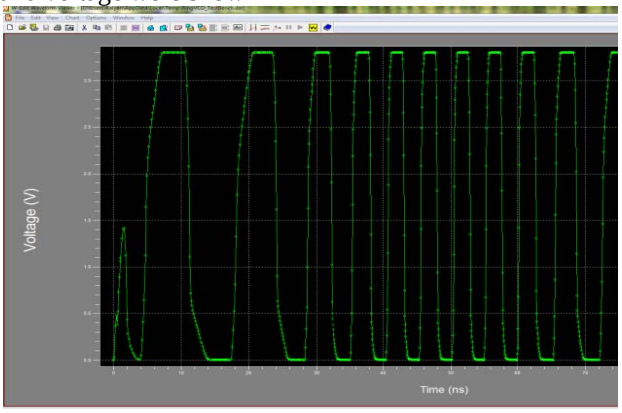


Figure11: Netlist window

V SIMULATION RESULTS

The simulation results of schematic of the crystal oscillator is shown in the below figure. The relationship between time and voltage were shown



CONCLUSION

The ESD-Protected On-Chip Crystal oscillator covers all the aspects like Perfect Matched Layout, Robust ESD Performance On Output Pins, Highly Stable Oscillations, Less parasitic resistance and capacitance on chip. The layout of the crystal oscillator is drawn with zero DRC errors which is ready to use for the fabrication.

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